Design and Modeling of a CNT-CMOS Low-Power Sensor Chip

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***Abstract*— Multi-walled carbon nanotubes (MWCNTs) has proved to be good sensing elements for many purposes including flow variations sensing and chemical vapor sensing. However, they are not used in real applications due to the cost and size of the complex equipments required to measure the response of MWCNTs. We proposed a novel methodology to integrate MWCNTs sensors on commercial Complementary Metal-Oxide Semiconductor (CMOS) processed chips using dielectrophoresis (DEP). The response of MWCNTs sensors will be measured by CMOS circuit on the same substrate. Using our proposed methodology, a low cost, compact and ultra-low power MWCNTs sensor could be built and ready for commercial applications. In this paper, we will discuss the issues on MWCNTs resistance measurement and integration of MWCNTs sensing elements - issues that will critically affect the design of the circuit components on the CMOS chip. A 0.35um CMOS prototype will be made to demonstrate the feasibility of such CNT-CMOS integration. Simulation results and implementation details will be given.**

***Index Terms*— CNT-CMOS Integration, NEMS, CNT Sensors, ultra-low power sensor**

I. Introduction

Since Carbon Nanotubes (CNTs) were discovered in 1991, researchers have found various interesting mechanical, electrical, and chemical properties about CNTs. Among those properties, the sensing ability of CNTs against chemical and flow variations has received considerable attention because of the CNTs outstanding response [1], [2]. Generally, MWCNTs based chemical and flow sensors have the advantages of small size, low power consumption (<1uW input on sensor), quick response, and high sensitivity compared with traditional sensors [2]. Hence our group has investigated several techniques to build CNT sensor in the past 3 years and have proved that batch fabrication of MWCNTs sensors is possible by using DEP and an automated microspotting system [3], [4].

To detect the response (resistance change) of a MWCNTs sensor, we could bias the MWCNTs resistor by a fixed current. However, owing to their minute dimensions, MWCNTs resistor is easily self-heated. To avoid the effect of self-heating during chemical vapor sensing, bias current should be kept small ($\sim 10uA$). In flow variation sensing applications, self-heating is necessary and the bias current should be much higher ($\sim 100uA$). Also, such self-heating effect is necessary in chemical sensor applications in removing attached chemical molecules. The voltage across the MWCNTs sensor may vary between $100mV$ to $2V$ in different bias currents. When small bias current is used, resistance measurement of MWCNTs sensor becomes difficult, and high accuracy current source and analogue to digital converter (ADC) are required to maintain a reasonable signal to noise ratio (SNR). Laboratory measuring equipments may be used to fulfill these constrains. However, commercialization of MWCNTs sensors is a great challenge due to the price and size of such measuring equipments.

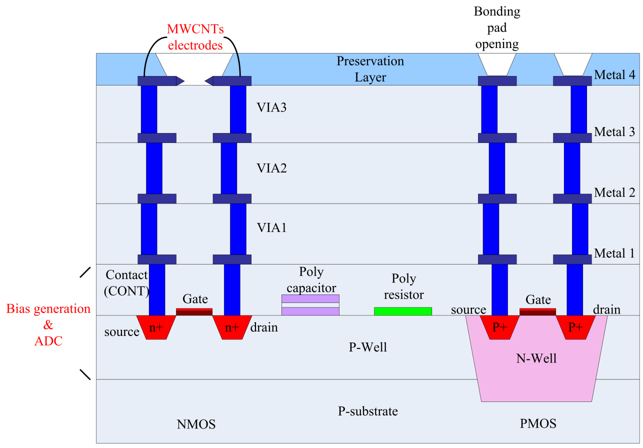

Fig. 1. Cross-sectional view of MWCNTs-CMOS integration.

II. MENS Integration of MWCNTs-CMOS sensor

To remedy the expensive and bulky equipment problem, we proposed a novel methodology that integrates MWCNTs sensors and all necessary measurement circuits within a single CMOS chip. We have chosen Austriamicrosystems (AMS) 0.35um CMOS process (S35D4) to implement our MWCNTs-CMOS sensor [5]. This is a 4 metals, 2 polys, single well process.

Due to the ease of fabricating MWCNTs sensors using DEP process, we may integrate MWCNTs sensor with the

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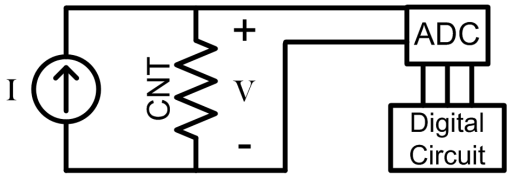

Fig. 2. System architecture of MWCNTs resistance measurement circuit.

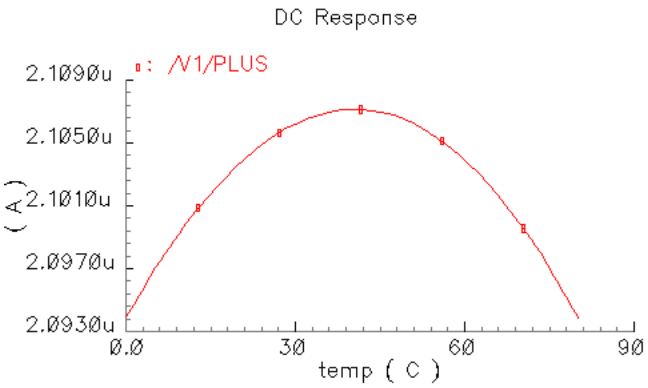

Fig. 3. Simulation result of temperature coefficient of master reference current

CMOS process by exposing some top metal structures on the wafer and fabricate MWCNTs sensor as a post-CMOS process. Some specially designed circuits are made within the same substrate using transistor, capacitor and resistor in the lower layers. These circuits generate the bias current for MWCNTs resistance measurement and the signal voltage of MWCNTs is read by a analogue to digital converter (ADC). The intermediate metal layers serve as the connection between MWCNTs sensor electrodes and the circuits. The cross-sectional diagram of the process and the location of MWCNTs electrodes, bias generation circuit and ADC circuit are illustrated in Fig. 1.

The advantages of our MWCNTs-CMOS integration are:

- The cost of making these CMOS circuits is low in large volume production. This can be achieved when we are commercializing the sensor. Single chip MWCNTs-CMOS integration eleminates expensive and bulky measurement equipment.
- Post-CMOS photolithography is avoided. The only post-CMOS operation to fabricate these sensors is DEP which can be automated easily [4]. Complicated CMOS process is done by the foundry.
- Signal distortion is avoided due to single chip implementation. Noise performance and sensitivity of MWCNTs sensor are enhanced.

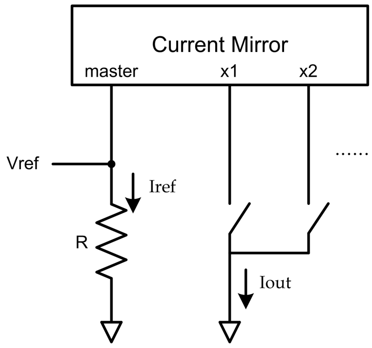

Fig. 4. Principle of programmable current source.

III. Circuit Implementation of MWCNTs-CMOS Sensor

A. System architecture

Our MWCNTs sensor-on-chip prototype consists of 3 major components, namely, electrodes for MWCNTs sensor formation, programmable current source and the analogue to digital converter.

Sensor electrodes are exposed on top metal structures with small separation ($\sim 5-10um$). They are connected to bonding pads of the chip and will be used for sensors formation using a post-CMOS DEP process. The programmable current source is responsible for providing a tiny fixed current (I) biasing the MWCNTs sensor at different operating regions, and the ADC is used to measure the signal voltage (V) developed across the sensor. At last, the resistive change of the sensor can be calculated from the measured (V) and programmed (I). Fig. 2 illustrates our system architecture.

B. Programmable bias current generation

To accommodate different bias current requirements for different applications, a programmable current source is constructed. A master reference current ($Iref$) is constructed by applying a reference voltage ($Vref$) to a V-to-I converter, and binary weighted current mirrors from x1 to x128 are used to make copy of master current. By controlling the switch on the tail of every current mirror, the output current ($Iout$) is controllable from 0 to 255 times of the ($Iref$) (see Fig. 4).

Resistor in normal CMOS process has lots of non-idealities. Specifically, two non-idealities may affect our construction of the current source. The first one is variation on absolute value of resistance (+/-20%), which occurs due to random error of etching and impurity doping level. The second one is the finite temperature coefficient of resistors. Both of these non-idealities can be reduced using trimming; however, trimming is time consumption and expensive.

Although the variation on absolute resistance value introduces a +/-20% variation on the value of master current (I_{ref}) and hence the absolute value of MWCNTs resistance measurement, it would not affect the operation of the sensor due to the fact that only relative percentage changes ($\Delta R/R$) of the sensors are of interest.

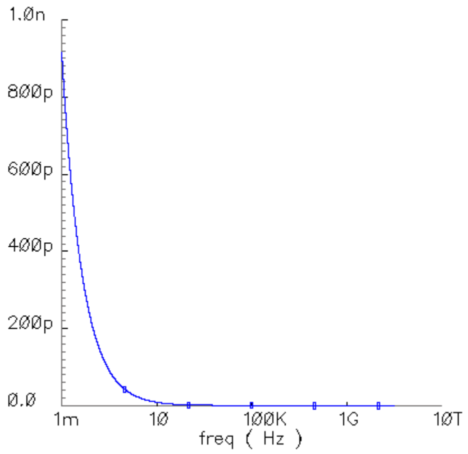

Fig. 5. Simulated output noise current of the programmable current source.

The problem of finite temperature coefficient of resistor is solved by making the reference voltage (V_{BG}) to have a temperature coefficient equal to that of resistor. Master current (I_{ref}) is thus temperature dependent according to the relation ($I_{ref} = V_{BG}/R$). Second order temperature coefficient mismatch makes a true zero temperature coefficient reference current (I_{ref}) impossible. Simulated result of our current source working at $2uA$ (in Fig. 3) shows that I_{ref} exhibits a 15ppm/K temperature coefficient. In real fabrication, process variation and mismatch in transistors and resistors exist, and may degrade the typical temperature coefficient to 15-70ppm from our prior experience.

The programmable current source is implemented and the schematic is shown in Fig. 9. A single stage folded cascade op-amp is used to construct the V to I converter due to noise and stability considerations. The base transistors of current mirrors (M1 and M4) are made large ($16um/12um$) to reduce $1/f$ noise. The output noise current of the current source is simulated from $1mHz$ to $100GHz$ and is shown in Fig. 5. The total output noise current is $0.941nA$ while the output signal current is 2uA, resulting in a $66dB$ SNR, which is high enough for our application.

It is also important to show that the output current (I_{OUT}) remains constant even in the change of MWCNTs resistance. The output current (I_{OUT}) versus output voltage (V_{OUT}) is simulated in Fig. 6. A 0.23ppm/mV dependence of (I_{OUT}) on (V_{OUT}) is observed, which means (I_{OUT}) only have a 0.023% change for every 1V change in (V_{OUT}). That result is good enough for our application. The layout of the programmable current source is shown in Fig. 7.

C. Analogue to digital converter

To maximize the sensitivity of MWCNTs sensors and keep power consumption minimum, noise from measuring circuit should be about the same value as the inherent noise of MWCNTs sensors [6]. We have investigate the inherent noise of MWCNTs sensors and found that a 60dB SNR in

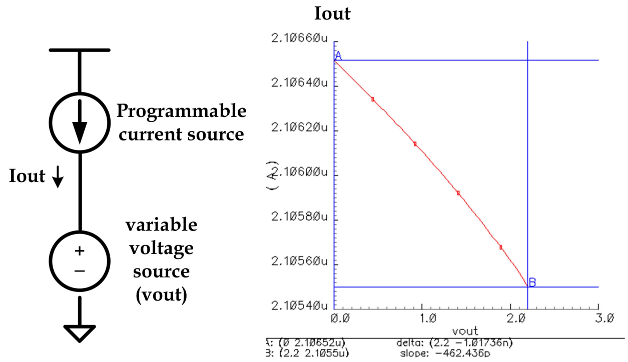

Fig. 6. Simulated dependence of I_{out} on V_{out}.

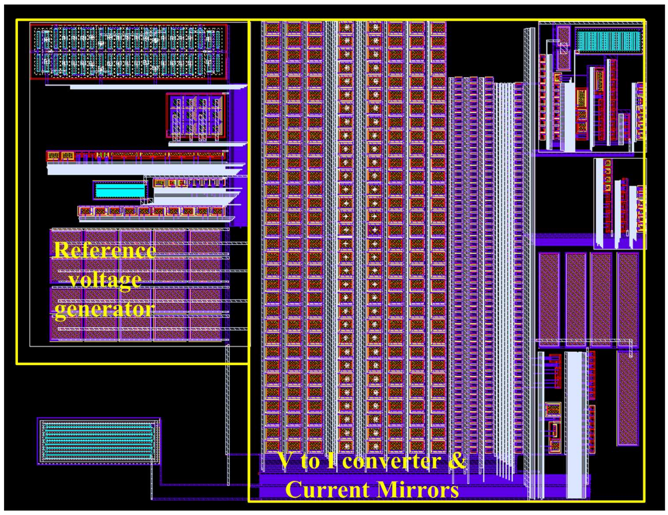

Fig. 7. Layout of the programmable current source.

voltage measurement is sufficient for alcohol sensing. By considering the lowest resistance ($10k$ohms) and lowest bias current ($10uA$) of MWCNTs sensors, we concluded that we need a 13-bit ADC to achieve a 60dB SNR (Eq. 1, 2):

$$Q_n = \frac{\Delta^2}{12} = \frac{(FSR/2^B)^2}{12} \tag{1}$$

$$SNR = 10log\frac{P_s}{Q_n} = 10log\frac{(I_B)^2 R_{CNT}}{Q_n} \tag{2}$$

where Q_n = quantization noise, Δ = size of quantization step, FSR = full scale range of ADC = 2.42, B = number of bit of ADC, P_s is power of signal voltage and I_B is bias current.

Without complex special calibration circuits, we can only achieve 13-bit accuracy using two classes of ADC, i.e., the *dual slope ADC* and *delta-sigma ADC*. Although delta sigma ADC was proven to be more power efficient in medium speed sampling rate, it requires complex digital circuits which occupy significant chip area. Our project aim is to demonstrate the feasibility of MWCNTs sensors and CMOS integration, hence we implemented a dual slope ADC to reduce the complexity and cost in our first CMOS prototype.

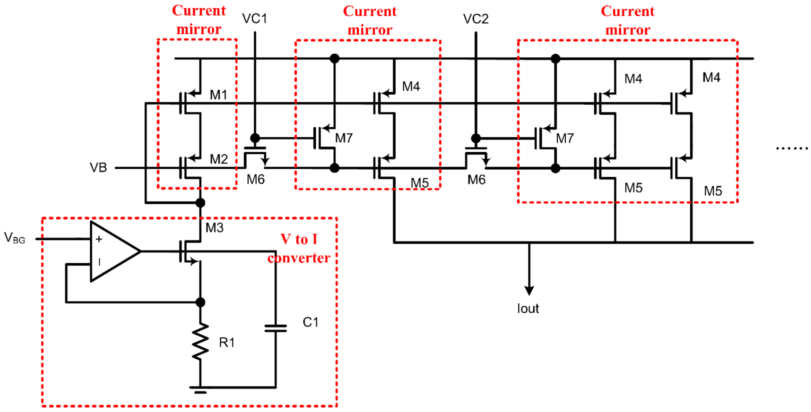

Fig. 9. Schematic of the programmable current source.

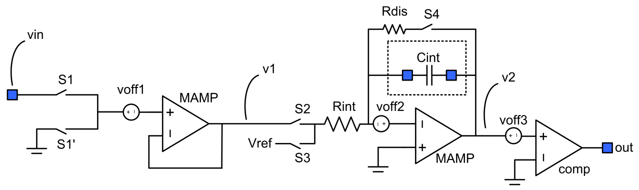

Fig. 8. Schematic of the ADC.

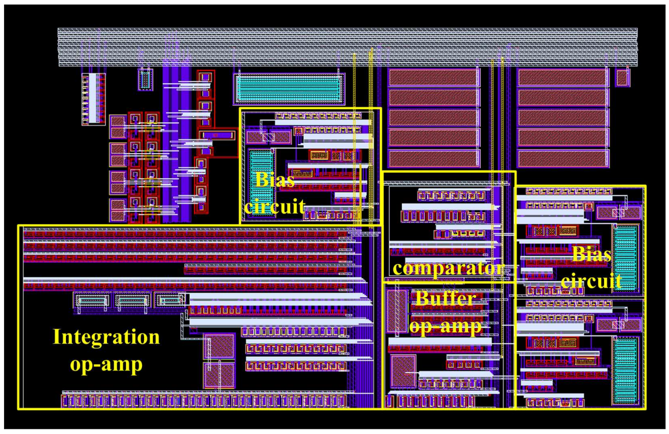

Fig. 10. Layout of the ADC.

The schematic of the dual slope ADC we implemented, including modeling of op-amp offset voltages, is shown in Fig. 8. The problem of unpredictable op-amp offset voltages is reduced by double conversion, and the offset of ADC code due to op-amp offset is sampled each time the system is started.

We have simulated every individual component of the ADC to ensure that their noise contributions are small enough to achieve a 13-bit accuracy. Some circuit non-idealities may also affect the accuracy of the ADC, which include finite signal dependent resistance of switches and charge injection problems introduce by the switches. We have simulated 20 V_{in} for the ADC and found the output have a 13-bit accuracy. However, the actual ADC we get from foundry may not be able to achieve a 13-bit accuracy due to the fact that some circuit non-idealities may not have been modeled by the foundry model and the external integration capacitor will have finite parallel resistance and dielectric absorption effect. To conclude, the accuracy of the ADC can be obtained only after we tested the fabricated CMOS chip. The layout of the ADC is shown in Fig. 10.

D. MWCNTs sensor electrodes

One of the most important features of our sensor chip is the single-chip-integration concept. Electrode pairs with 5-10um separation are required for MWCNTs sensors formation. Such resolution can be easily achieved in any metal layer in contemporary CMOS processes, but the resolution of creating openings on the protective layer (usually nitride layer) constrain the separation of electrode pairs to 15-20um. Such problem can be easily solved in production by requesting non-protected wafer from the foundry. In the current developmental stage, where multi-project on single wafer (MPW) fabrication service is used, we need specially designed structures and post-CMOS process to solve this problem.

We have prepared 3 different kinds of electrode pairs. The first one is the standardly exposed electrode pairs with 15um separation and require no post-CMOS process (Fig. 11). The second type is electrode pairs with 2um separation without protective layer opening (Fig. 12), i.e., post-CMOS photolithography and etching is necessary to make openings for these electrode pairs. At last, we prepared some wide top metal structures which serve as the base of electrodes. Post-CMOS photolithography and deposition processes will be used to make the electrodes on the top of it.

In this developmental stage, we cannot connect MWCNTs electrodes to resistance measurement circuit directly because those circuits cannot withstand high AC voltage ($20V_{p-p}$). Every MWCNTs electrode is connected to a bonding pad and external connection is used to connect those electrodes

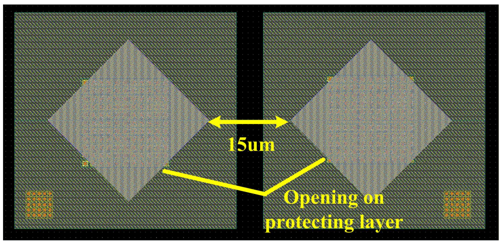

Fig. 11. MWCNTs electrodes with protective layer opening.

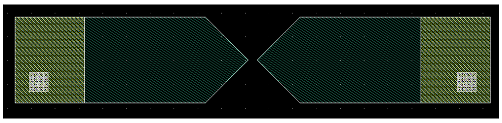

Fig. 12. MWCNTs electrodes without protective layer opening; post-CMOS process is required.

and the resistance measurement circuits. Special attention is also paid on the bonding pads. Bonding pads with ESD structures commonly used in other electronic components are not used for MWCNTs electrodes, i.e., these ESD pads cannot withstand high AC voltage during the sensor formation process; hence, bare bonding pads are used for the MWCNTs sensors. In production, we may use high voltage CMOS process so that the connections can be made internally at the price of higher cost.

IV. Conclusion

A novel idea that integrates MWCNTs sensors with a commercial CMOS process is presented. A prototype chip has been designed and is being fabricated by Austriamicrosystems using the S35D4 process (Fig. 13). We are expecting the prototype CNT-CMOS chip will show a low cost, compact and lower power consumption for sensor-on-chip applications.

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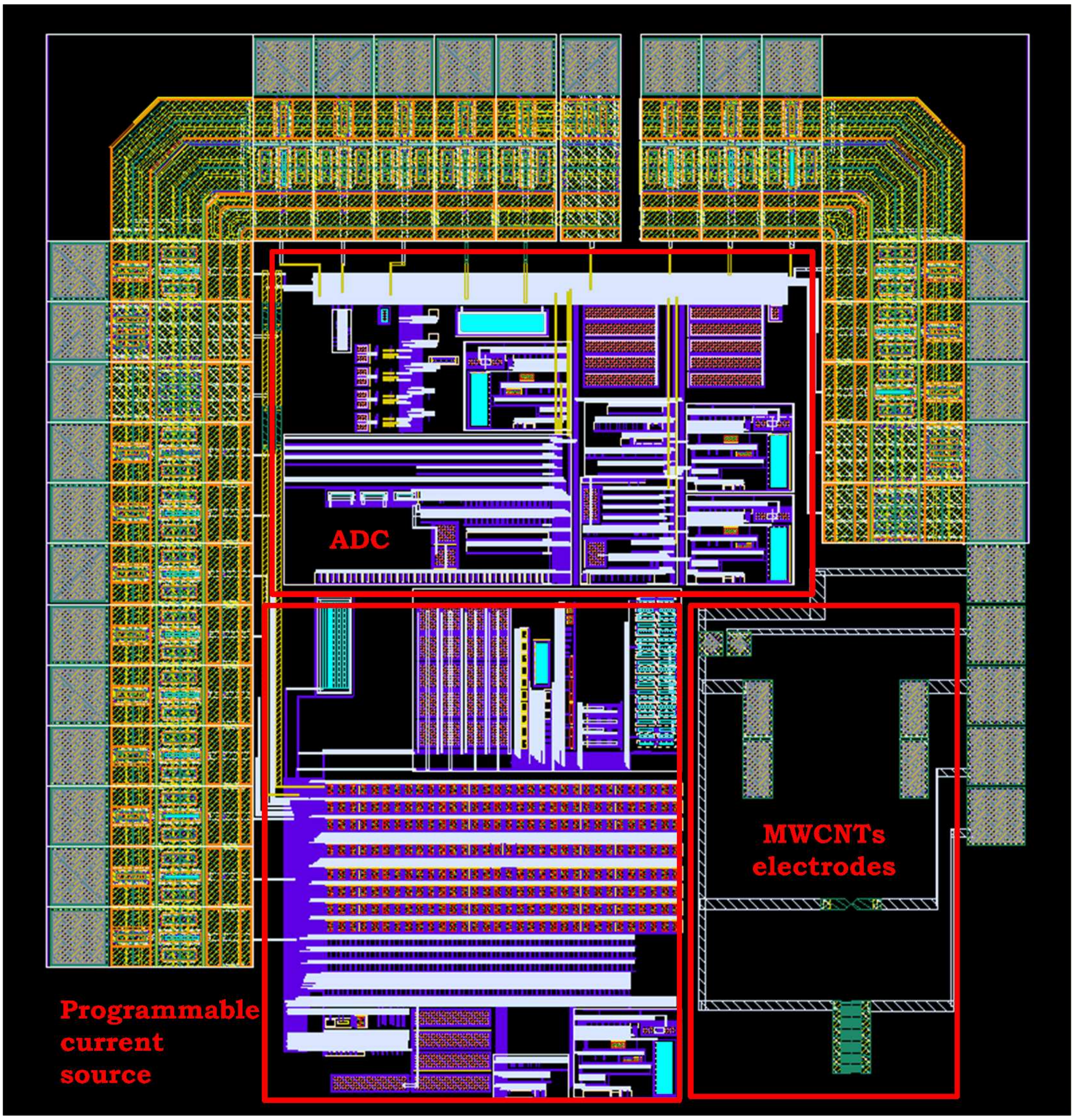

Fig. 13. Layout of CMOS-MWCNTs sensor chip prototype.